AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [1029] with the following amended paragraph:

[1029] Although INIT may be received from an input/output pin, this signal may be generated on-chip by voltage initialization circuit 170. An exemplary voltage initialization circuit 170 is illustrated in FIG. 4. Voltage initialization circuit 170 is coupled to initialize a single illustrative latch 430. When INIT is high, transistors 420 and 428 are effectively enabled and node 424 is charged or discharged according to selective connectors 422 and 426, respectively. Typically, only one of n-type transistor 428 and p-type transistor 420 may be present or may be effectively coupled to node 424 for a given latch. Selective ~~connectors 420 and 426~~ connectors 422 and 426 may be fuses, anti-fuses, or any other suitable device. When INIT is low, n-type transistor 428 and p-type transistor 420 are effectively disabled and node 424 receives data according to the clock signal.